

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	13	("20020099893" "20020120801" "5729760" "5796984" "6209083" "6272618" "6282601" "6480914" "6571206" "6636962").PN. OR ("6711642").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/05/10 06:20
L2	0	"2003028781"	US-PGPUB; USPAT; USOCR	OR	OFF	2007/05/10 06:20
L3	1	"20030028781"	US-PGPUB; USPAT; USOCR	OR	OFF	2007/05/10 06:33
L4	2	("6832317").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/10 06:33
L12	38	("4819234" "5175853").PN. OR ("5357628").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/05/10 07:08
S87	277	714/34.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:43
S88	13	714/34.ccls. and smi	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:44
S89	38	("4819234" "5175853").PN. OR ("5357628").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/10/19 13:38
S90	38	("4819234" "5175853").PN. OR ("5357628").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/10/19 14:59
S91	14	("4953084" "5047926" "5053949" "5357628" "5394544" "5471620" "5701488").PN. OR ("6249881").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/10/19 13:45

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S92	26	("4674089" "4782461" "5175853" "5182811" "5228039" "5313618" "5321828" "5339437" "5357628" "5392420" "5410710" "5437039" "5539901").PN. OR ("5682310"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/10/19 15:01
S93	870	714/30.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/05/09 13:43
S95	10	S93 and smi	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:44
S96	2	S93 and (system adj management adj interrupt)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/19 14:36
S97	8	S88 and (system adj management adj interrupt)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/19 14:41
S98	310	714/31.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/19 14:41
S99	4	714/31.ccls. and smi	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:43
S10 0	3	714/31.ccls. and (system adj management adj interrupt)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/19 14:43
S10 1	5	S90 and chipset	US-PGPUB; USPAT; USOCR	OR	OFF	2006/10/19 14:59
S10 3	7	714/30.ccls. and (chipset and interrupt)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/10/19 15:05

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S10 4	5	714/34.ccls. and (chipset and interrupt)	US-PGPUB; USPAT; USOCR	OR	OFF	2007/05/09 13:16
S10 5	13	714/31.ccls. and (chipset and interrupt)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/10/19 15:06
S10 6	3	((south-bridge) adj chipset) and interrupt)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/10/19 15:07
S10 7	3	((south-bridge) adj chipset) and interrupt)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/19 15:08
S10 8	1	((south-bridge) adj chipset) and smi)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/31 13:40
S10 9	5	((south adj bridge) adj chipset) and smi)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/19 15:09
S11 0	5	((south adj bridge) adj chipset) and (system adj management adj interrupt))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/19 15:10
S11 1	202	((south adj bridge)) and smi)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/31 13:41

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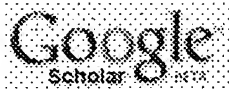
S11 2	72	((south adj bridge)) with smi)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/31 13:43
S11 3	0	((south adj bridge)) with smi) with debug\$5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/31 13:43
S11 4	11	((south adj bridge)) with smi) and debug\$5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:33
S11 5	356	debug\$5 and smi	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/12 12:38
S11 6	4	07/858,301	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/12 12:33
S11 7	11	"858,301"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/12 12:33
S12 2	174	debug\$5 and smi and window	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/12 12:38
S12 3	22	("6968410") or ("6711642") or ("6636962") or ("6571206") or ("6480914") or ("20020099893") or ("6282601") or ("6272618") or ("6209083") or ("5796984") or ("5729760")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:20

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S12 4	1	10/820768	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:22
S12 5	2	S123 and debug\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:22
S12 6	0	((south adj bridge)) with smi with debug\$5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:33
S12 7	2	((south adj bridge)) and (smi with debug\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:45
S12 8	10	((bridge)) and (smi with debug\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:34
S12 9	296	714/34.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:43
S13 0	970	714/30.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/05/09 13:43
S13 1	296	714/34.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:43
S13 2	5	714/31.ccls. and smi	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:43

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S13 3	13	714/34.ccls. and smi	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:44
S13 4	970	714/30.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/05/09 13:44
S13 5	11	S134 and smi	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:44
S13 6	30	((south adj bridge)) and (smi and debug\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:45
S13 7	204	((bridge)) and (smi and debug\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/09 13:49



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Device for **debugging** and method thereof

CC Huang, HL Lin - 2005 - freepatentsonline.com

... operation window for users to **debug** when CPU is ... design becomes easier, and the **debugging** procedure becomes ... bridge Chipset [0025] 14 **south-bridge** Chipset [0026 ...

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Increasing the number of I/O decode ranges using **SMI** traps

M Rangarajan, S Gupta - 2006 - freepatentsonline.com

... referred to as a super I/O controller, is also preferably coupled to **Southbridge** chipset 50 ... The **debug** operation may further allow **debugging** programs to ...

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Method and apparatus for emulating an OS-supported communication device to enable remote **debugging**

TF Emerson, D Heinrich, CJ Frantz, A Brown - 2003 - freepatentsonline.com

... an OS-supported communication device to enable remote **debugging**. ... from an SIO to a **southbridge**, to alter ... which is typically located in a **south bridge** portion of ...

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PROCESSOR WITH PROTECTED TEST AND DEBUG MODE - all 2 versions »

GS STRONGIN - EP Patent 1,410,143, 2004 - freepatentsonline.com

... to store one or more hardware-**debug**-test (HDT ... signal from the power supply, the **south bridge** (or north ... asserting a system management interrupt (**SMI**) signal, in ...

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Transmeta Crusoe

PP Series, L Harrison - cs.uiuc.edu

... & **Southbridge** Interface Page 15. CS433 Prof. Luddy Harrison Copyright 2005 University of Illinois 15 64 General Purpose Registers Shadow Registers **Debug** Reg ...

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Cache with finely granular locked-down regions - all 3 versions »

DW Green - US Patent 6,044,478, 2000 - Google Patents

... MSRO MSR3 CONTROL REGISTERS DESCRIPTOR TABLE REGISTERS TASK REGISTER **DEBUG** REGISTERS CONFIGURATION REGISTERS MODEL SPECIFIC REGISTERS TEST REGISTERS Page 4. ...

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XpressROM: Geode™ Technology Software - all 2 versions »

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... I **SMI** (System Management Interrupt) -Based Memory Access Capability — An **SMI** handler feature useful for **debugging** in unfamiliar or highly protected ...

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System and method for logging hardware usage data, and uses for such logged hardware usage data

H Hodge, GL Stephens - 2006 - freepatentsonline.com

... and third level support in **debug** efforts regarding ... **South bridge** 104 is also communicatively coupled to ... calls, System Management Interrupt (**SMI**), ASL, SMBios ...

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Message based power management - all 2 versions »

DE Gulick, FP Helms, LD Hewitt, WA Hughes, PC ... - US Patent 7,051,218, 2006 - Google Patents

... (I/O) hub 204 provides much of the functionality provided in prior art systems by the **south bridge** component of the chipset supporting processor operations. ...

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Use of a signal line to adjust width and/or frequency of a communication link during system ... - all 2 versions »

»

FP Helms, DR Meyer, LD Hewitt, DE Gulick, WA ... - US Patent 7,146,510, 2006 - freepatentsonline.com

... Logic 0s are recommended for easier **debug**. ... The I/O hub (or **south bridge** according to the particular ... the order in which STPCLK and **SMI** system management ...

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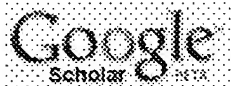
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... in step 20, the users trigger the **south-bridge** chipset 14 ... operation window for users to **debug** when CPU ... of **debugging** [0020] The device for **debugging** and method ...

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P Features - jameco.com

... PIIX4E **South Bridge** ... Normal state is made by a halt break event (one of the following signals going active: NMI, INTR, BINIT#, INIT#, RESET#, FLUSH#, or SMI#). ...

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